Q.P. Code: **18CS0505** **R18**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Regular Examinations Nov/Dec 2019

COMPUTER ORGANIZATION & ARCHITECTURE

(CSE & CSIT)

Time: 3 hours Max. Marks: 60

PART-A

(Answer all the Questions **5 x 2 = 10** Marks)

1	**a**	Define MAR.	**2M**
	b	Define Fixed-point representation.	**2M**
	c	What are the arithmetic micro operations?	**2M**
	d	Differentiate between SRAM & DRAM.	**2M**
	e	Define pipelining.	**2M**

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	**a**	Write bout Registers.	**5M**
	b	Write bout instruction set.	**5M**
		OR	
3		Write in detail about the Functional Units of Computer with neat diagram.	**10M**

UNIT-II

4	**a**	Write about hardwired control unit.	**4M**
	b	Write the Booth multiplication algorithm and Draw the flowchart.	**6M**
		OR	
5		Show the step-by-step signed-operand multiplication process using Booth algorithm.	**10M**

UNIT-III

6		Explain about Micro Programmed Control with neat sketch.	**10M**
		OR	
7	**a**	Show that the block diagrams of the hardware that implements the following register transfer statement P: R2←R1.	**6M**
	b	Explain the way of constructing a 4-line common bus system with a neat diagram.	**4M**

UNIT-IV

8		Describe the use of DMA controllers in a computer system with a neat block diagram.	**10M**
		OR	
9	**a**	Explain about Memory Hierarchy.	**6M**
	b	Explain about Memory Management Requirements.	**4M**

UNIT-V

10	**a**	Explain about Parallel Processing and its Types.	**6M**
	b	Explain the concept of Pipelining with clear example with neat sketch.	**4M**
		OR	
11	**a**	Write about hyper cube network with neat sketch.	**5M**
	b	Write about multistage network with neat sketch.	**5M**

END